What is claimed is:

1. An apparatus for display of video data from a designated number of an N number of video channels, the apparatus comprising:

an N number of video decoders to receive the video data from the N number of video channels, a designated number of the N number of video decoders to decode the video data from the designated number of the N number of video channels; and

a P number of video processing pipelines coupled to the N number of video decoders through a switch network, the switch network configured to connect any of the outputs from the N number of video decoders to any of the inputs into the P number of video processing pipelines.

2. The apparatus of claim 1, further comprising an image size/location logic to receive a designated size of a display window and the designated number of the N number of video channels whose video data is to be displayed in the display window, the image size/location logic to determine a location in the display window and a size of a part of the display window for display for the video data for each of the designated number of video channels.

3. The apparatus of claim 2, further comprising N number of scalers, wherein a designated number of the N number of scalers are to scale the decoded video data from the designated number of the N number of video channels based on the determined size of the part of the display window.

4. The apparatus of claim 1, wherein the P number of video processing pipelines are to process the decoded video data of the designated number of the video channel received from the designated number of the N number of video decoders.

5. The apparatus of claim 4, wherein P is less than N and wherein the apparatus further comprises a display/control logic to control a process order of the designated number of the N number of video channels by the P number of video processing pipelines.

6. The apparatus of claim 1, further comprising a write multiplexer to receive the processed decoded video data from the P number of video processing pipelines, the write multiplexer to store the processed decoded video data from the designated number of the N number of video channels into a memory.

7. A method for displaying video data from N number of video channels in a display, the method comprising:

decoding, with N number of video decoders, a part of video data received in N number of video channels;

inputting the decoded part of the video data into P number of video processing pipelines through a switch network; and

processing, by the P number of video processing pipelines, the decoded part of the video data in the N number of video channels.

8. The method of claim 7, wherein P is less than N.

9. The method of claim 7, further comprising storing the processed decoded part of the video data in the N number of video channels into a part of a video buffer that is not updating the display.

10. The method of claim 9, further comprising switching the part of the video buffer that is not updating the display with a part of the video buffer that is updating the display,

upon determining that the P number of video processing pipelines has completed processing the decoded part of the video data for each of the N number of video channels.

11. The method of claim 7, wherein decoding, with the N number of video decoders, the part of video data received in the N number of video channels comprises decoding, with the N number of video decoders, a frame in the video data received in the N number of video channels.

12. The method of claim 7, wherein decoding, with the N number of video decoders, the part of video data received in the N number of video channels comprises decoding, with the N number of video decoders, a field of a frame in the video data received in the N number of video channels.

13. The method of claim 7, wherein decoding, with the N number of video decoders, the part of video data received in the N number of video channels comprises decoding, with the N number of video decoders, a scaled field of a frame in the video data received in the N number of video channels.

14. A method comprising:

receiving an image size and a location in a display;

receiving a designated number of an N number of video channels to be displayed in the image; and

performing the following for each of the designated number of the N number of video channels:

decoding, with one of an N number of video decoders, a frame of video data received in the video channel;

inputting the decoded frame into one of a P number of video processing pipelines through a non-blocking switch network;

processing, by the one of the P number of video processing pipelines, the decoded frame; and

storing the processed decoded frame into a part of a video buffer that is not updating the display.

15. The method of claim 14, wherein processing, by the one of the P number of video processing pipelines, the decoded frame comprises determining whether the video channel is in a failed state.

16. The method of claim 15, wherein processing, by the one of the P number of video processing pipelines, the decoded frame comprises outputting a blacked out frame for the video channel upon determining that the video channel is in a failed state.

17. The method of claim 14, further comprising switching the part of the video buffer that is not updating the display with a part of the video buffer that is updating the display, upon determining that the P number of video processing pipelines has completed processing the decoded frame for each of the designated number of the N number of video channels.

18. The method of claim 14, wherein performing the following for each of the designated number of the N number of video channels further comprises scaling the decoded frame based on the image size and the designated number of the N number of video channels.

19. A system for displaying video data from a designated number of N number of video channels on a video display terminal, the system comprising:

an N number of video sources, wherein each of the N number of video sources is to generate video data in a video channel of the N number of video channels; and

a video logic comprising:

an N number of video decoders, wherein each of the N number of video decoders is to receive the video data from one of the N number of video channels and to decode the video data; and

a P number of video processing pipelines coupled to the N number of video decoders through a switch network, the switch network configured to connect any of the outputs from the N number of video decoders to any of the inputs into the P number of video processing pipelines, wherein one of the P number of video processing pipelines is to process the decoded video data from one of the N number of video decoders.

20. The system of claim 19, wherein the video logic further comprises an image size/location logic to receive a control input for a size and a location of a window in the video display terminal and the designated number of the N number of video channels to display in the window, wherein the image size/location logic is to determine a location in the window and a size of a part of the window for display for the video data for each of the designated number of video channels.

21. The system of claim 20, wherein the video logic further comprises an N number of scalers, wherein each of the N number of scalers is to scale the decoded video data from one of the N number of video channels based on the size of the part of the window determined by the image size/location logic.

22. The system of claim 19, wherein P is less than N and wherein the video logic further comprises a display/control logic to control an order of processing of the decoded video data in the designated number of N number of video channels by the P number of video processing pipelines.

23. The system of claim 19, wherein the one of the P number of video processing pipelines is to execute a video fail operation if the one of the N number of video decoders does not lock onto the video data from the one of the N number of video channels after a predetermined time.

24. The system of claim 23, wherein the video fail operation comprises an output of a blacked out frame overlaid with a descriptive text to indicate video failure for the one of the N number of video channels.

25. The system of claim 23, wherein the video fail operation comprises an output of a previous image for the one of the N number of video channels overlaid with a descriptive text to indicate video failure.

26. The system of claim 19, wherein the video data is analog video data.

27. The system of claim 19, wherein the video logic further comprises a write multiplexer coupled to the P number of video processing pipelines, wherein the write multiplexer is to write the processed decoded video data from the P number of video processing pipelines into a video buffer.

28. The system of claim 27, wherein the video logic further comprises a clock multiplier network, the clock multiplier network to control a rate of operation of the write multiplexer.

29. The system of claim 27, wherein the rate of operation is approximately at least P/2.